METHODS AND APPARATUS FOR IMPROVING CRITICAL PATH ANALYSIS

USING GATE DELAY

Abstract of Invention

Disclosed are novel methods and apparatus for efficiently providing critical path

analysis of a design. In an embodiment, an apparatus disclosed can assist in creating a

single critical path schematic which can be used to simulate both rising and falling edge

delays. This saves time as only one schematic and one simulation is required instead of

the two generally required.

Docket No.: 5858.P7166C

Express Mail No.: EL962312158US